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DEVICE AND CIRCUIT LEVEL SIMULATION STUDY OF NOR GATE LOGIC FAMILIES DESIGNED USING NANO-MOSFETs

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ABSTRACT

The investigation of silicon-based nano-MOSFETs logic circuits is helpful to gain more comprehensive knowledge about nanoscale transistors. Therefore, a simulation study has been performed on four logic families of two inputs NOR gate logic circuits, namely (i) nano-CMOS NOR gate, (ii) nano-MOSFET loaded n-type nano-MOSFET NOR gate, (iii) 733.8 Ω resistive loaded nano-MOSFET NOR gate, and finally (iv) pseudo-n-type nano-MOSFET NOR gate. The nano-MOSFET technology node studied in this paper is 10 nm. Device simulation is done using an online NanoMOS simulator, whereas circuit simulation is carried out using freeware WinSpice. The main obstacle encountered during downscaling of nano-MOSFETs is low power dissipation and high-speed nano-MOSFET logic circuits. Correct logical NOR operation has been proven by observing simulated timing waveforms. Transient timing analysis on nano-MOSFET loaded n-type nano-MOSFET NOR gate has shown that propagation delays calculated from theory and simulation are 66% matched. From the analysis, this 10 nm nano-MOSFET NOR logic circuit design exhibit a dynamic power reduction of 148 times and a propagation delay improvement of 33 times when benchmarked against a typical 120 nm MOSFET logic circuit.

***Keywords**: nano transistor, electrical characteristics, channel length, channel width, benchmarking, power, speed*

INTRODUCTION

Over the past few decades, downscaling of MOSFET from micrometer regime to nanometer regime has occurred rapidly [1-8]. A research study on a 4 nm nano-MOSFET device is reported in the literature [9]. However, in this mentioned research, the oxide material is Hafnium Oxide (HfO_2), and the semiconductor material is Indium Gallium Arsenide (InGaAs). Therefore, this 4 nm nano-MOSFET is unsuitable for manufacturers to use Silicon-based fabrication facilities. This paper is devoted to studying electrical performance (such as propagation delay and power dissipation) of 10 nm Si-based nano-MOSFET [10]-[12]. To enable the gate to control the charge in the channel, the requirement $T_{ox} << L$ must be fulfilled, where T_{ox} is the oxide dielectric thickness. In this paper, the gate oxide thickness is about 1.5 nm which means that the oxide insulator is few atoms thick.

Four different logic families, namely (i) nano-CMOS NOR gate, (ii) nano-MOSFET loaded n-type nano-MOSFET NOR gate, (iii) 733.8 Ω resistive loaded nano-MOSFET NOR gate, and lastly (iv) pseudo-n-type nano-MOSFET NOR gate have been investigated in this paper. To counter-balance, the difference in carriers (electron and hole) mobility, circuit (i) has NMOS with a channel length, L=10 nm, and channel width, W = 125 nm, whereas PMOS has L = 10 nm and W = 250 nm. Circuit (ii) has NMOS L = 10 nm and W = 250 nm, whereas NMOS load width (W) and length (L) are 125 nm and 10 nm, respectively. Circuit (iii) has a 733.8 Ω resistive load, and its NMOS has a width (W) and length (L) equal to 250 nm and 10 nm, respectively. Circuit (iv) has NMOS with L = 10 nm and W = 250 nm, whereas PMOS has L = 10 nm and W = 125 nm. A constant field scaling technique has been adopted [13]. Electrical performance in terms of power dissipation, rise time, fall time, propagation delay, and maximum operating frequency has been

analysed and benchmarked against another research report [14-18]. From the report written by Kousik [19], the benchmarked MOSFET has a device dimension of V_{DD} = 2.0 V, T_{Si} = 60 nm, L = 120 nm, and W = 1 µm.

METHODOLOGY

NanoMOS, an online nano device simulator tool developed by Purdue University, has been used to performed device simulation. After this step, all these four NOR gate Spice circuit file codes are simulated using freeware WinSpice. The WinSpice simulation output consists of input timing diagrams and output timing diagrams. Two input signals with periods 10 ns and 20 ns are used to test the NOR gates. The transient response, which includes rise time, fall time, propagation delay, and maximum operating frequency, is simulated and analysed with 10 ps and 20 ps. The nano-MOSFET device design simulated using NanoMOS is shown in Figure 1. By performing this online device simulation, current-voltage (I-V) curves (refer to Figure 2 and Figure 3) and device parameters (refer to Table 1) are obtained, which are used to derive the timing response for nano-MOSFET loaded nano-MOSFET NOR logic circuit (refer to Table 2) [20-24]. Device structural dimensions in Table 1 are in the nanometer regime, which is compatible with silicon lattice constant of 0.5431 nm. This condition

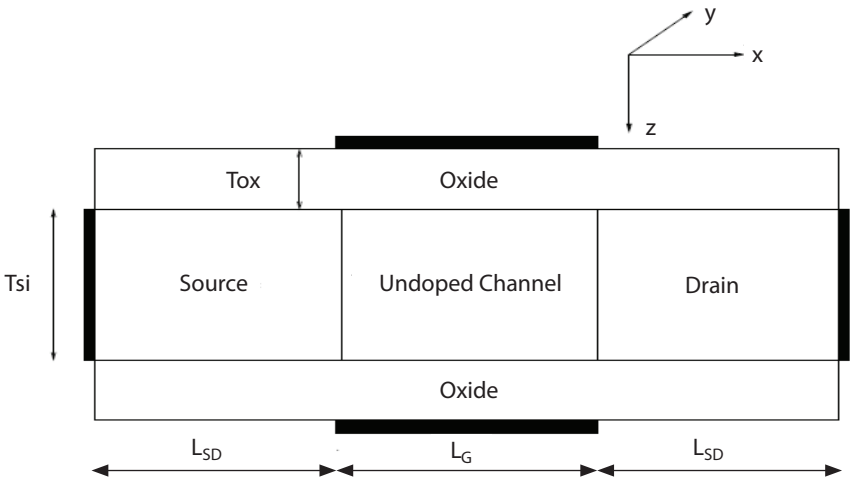


Figure 1 Nano-MOSFET structure used in NanoMOS online simulation

Table 1 Structural dimension of nano-MOSFET

Double Gate nano-MOSFET Device Simulation Parameters	
V_{GS}	0.60 V
V_{DS}	0.60 V
V_T	0.20 V
Source/Drain Doping Concentration (N_D)	1×10^{20} cm^{-3}
Channel Body Acceptor Impurity Concentration (N_A)	1×10^{16} cm^{-3}
Channel Width (W)	125 nm
Channel Length (L)	10 nm
Source Length/Drain Length (L_{SD})	7.5 nm
Silicon Channel Thickness (T_{Si})	1.5 nm
Top/Bottom Oxide Insulator Thickness (T_{OX})	1.5 nm
Top/Bottom Insulator Relative Dielectric Constant	3.9
Channel Body Relative Dielectric Constant	11.7
Top/Bottom Gate Contact Work Function	4.188 eV

Table 2 Theoretical modelling calculation values of nano-MOSFET loaded nano-MOSFET NOR gate

Double Gate nano-MOSFET Loaded NOR Gate	
Gate Capacitance (C_G)	5.755×10^{-17} F
Area Capacitance (C_A)	1.612×10^{-19} F
Sidewall Capacitance (C_{SW})	6.072×10^{-17} F
Drain Capacitance (C_D)	4.604×10^{-18} F
Source Capacitance (C_S)	1.046×10^{-17} F
nano-MOSFET Loaded Resistance (R_{Load})	733.8 Ω
nano-MOSFET on-state Resistance (R_{on})	36.2 Ω
Loaded NOR2 Gate Total Capacitance (C_{total})	1.381×10^{-16} F
Rise Time Constant (τ_r)	1.013×10^{-13} s
Rise Time (t_r)	1.360×10^{-12} s
(i) Best Case when 2 nMOS Turn On	
Fall Time Constant (τ_f)	2.499×10^{-15} s
Fall Time (t_f)	5.499×10^{-15} s
Propagation Delay (t_p)	3.598×10^{-14} s
Maximum Signal Frequency (f_{max})	7.323×10^{11} Hz
(ii) Worst Case when 1 nMOS On and 1 nMOS Off	
Fall Time Constant (τ_f)	4.999×10^{-15} s
Fall Time (t_f)	1.099×10^{-14} s
Propagation Delay (t_p)	3.685×10^{-14} s
Maximum Signal Frequency (f_{max})	7.293×10^{11} Hz

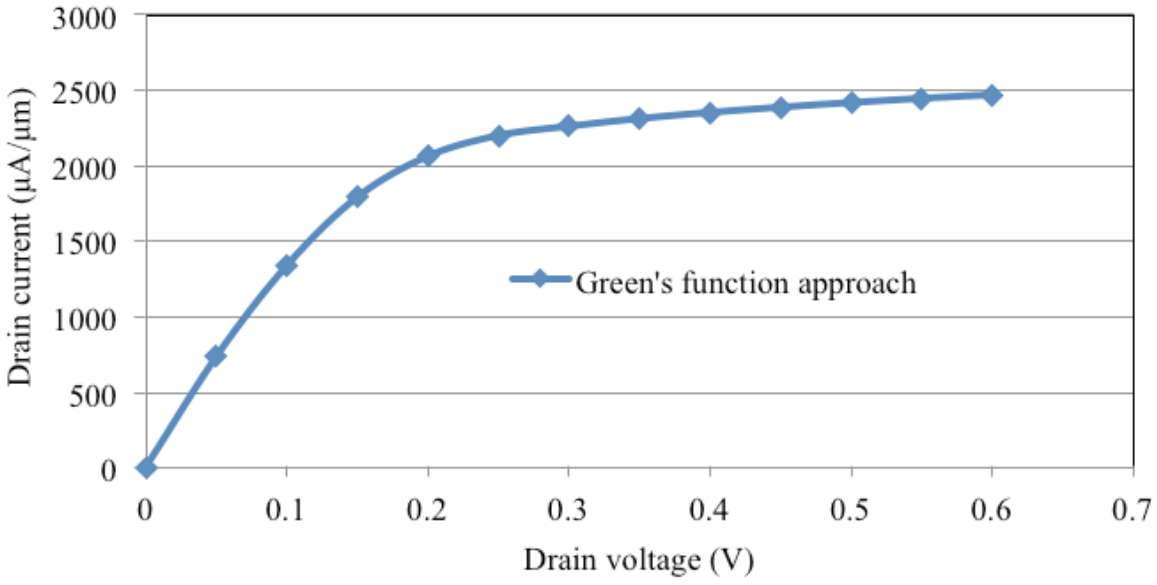


Figure 2 Drain current – drain voltage curve of nano-MOSFET with V_{GS}=0.60 V

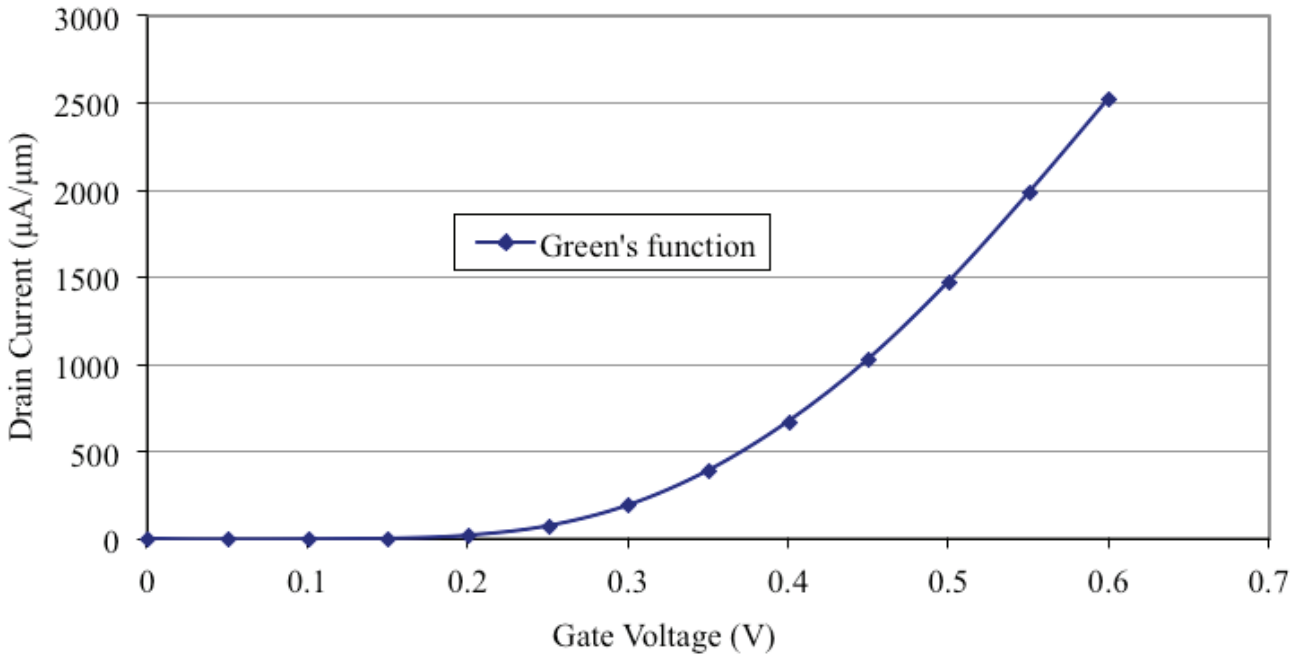


Figure 3 Drain current – gate voltage curve of nano-MOSFET with V_{DS}=0.60 V

causes electron quantum transport mechanism. Table 3 shows PMOS structural simulation parameter settings with a metal gate made from Aluminium. The logical NOR gate truth table is tabulated in Table 4.

Table 3 PMOS structural dimension

PMOS Device Simulation Parameters	
V_T	–0.15 V
Oxide Insulator Thickness (T_{OX})	1.5 nm
Channel Width (W) (for CMOS Logic)	250 nm
Channel Width (W) (for Pseudo Logic)	125 nm
Channel Length (L)	10 nm
Gate Capacitance (C_G)	6.852×10^{-17} F
Drain Capacitance (C_D)	7.29×10^{-17} F
Source Capacitance (C_S)	7.29×10^{-17} F

Table 4 Truth table for NOR logic gate

Inputs		Output
in1	in2	out1
0	0	0
0	1	1
1	0	1
1	1	1

Theories, expressions, and equations which are used to derive data in Table 2 are listed below. The drain current per micro width is written as

$$\frac{I_D}{W} = BC_{ox}\tilde{v_T}\,(V_{GS} - V_T)\left[\frac{1-\dfrac{\mathcal{F}_{1/2}\left(\eta_{F1}\dfrac{qV_D}{k_BT}\right)}{\mathcal{F}_{1/2}(\eta_{F1})}}{1+\dfrac{\mathcal{F}_0\left(\eta_{F1}\dfrac{qV_D}{k_BT}\right)}{\mathcal{F}_0(\eta_{F1})}}\right] \quad (1)$$

where the ballistic efficiency is B, the oxide capacitance is C_{ox}, the thermal velocity is $\tilde{v_T}$ and Fermi-Dirac integrals of order ½ and zero are used. η_{F1} is obtained from the subband energy profile of the nano-MOSFET. All nano-MOSFETs worked in saturation region with conditions $V_{GS} > V_T$ and $V_{DS} > V_{GS} - V_T$, except the load transistor of nano-MOSFET loaded n-type nano-MOSFET NOR gate which operated in resistive region with value R_{Load}.

$$R_{Load} = \frac{V_{th}}{I_{on\text{-}state\ at\ linear\ region} \times W} \quad (2)$$

Since digital logic gates operate at a linear portion of the I-V curve,

$$R_{channel\ at\ on\text{-}state} = \frac{1}{\mu_n C_{OX}(V_{DD} - V_T)} \quad (3)$$

where μ_n is the electron ballistic mobility.

Total Capacitance at Output Node in NOR logic (C_{total}) = Gate Capacitance + Area Capacitance + Sidewall Capacitance + (2 × Drain Capacitance) + Source Capacitance

$$\text{Rise time constant } (\tau_r) = R_{\text{Load}} \times C_{\text{total}} \quad (4)$$

$$\text{Rise time } (t_r) = 2.2 \times \tau_r \times 6.1 \quad (5)$$

It takes 6.1 times duration to pass logic 1 than logic 0 through an *n*-channel MOS pass transistor.

(i) Best case when 2 *n*-MOS Turn on

$$\text{Total } R_{\text{on}} = (R_{\text{Channel on-state}})/2 \quad (6)$$

$$\text{Fall time constant } (\tau_f) = \text{Total } R_{\text{on}} \times C_{\text{total}} \quad (7)$$

$$\text{Fall time } (t_f) = 2.2 \times \tau_f \quad (8)$$

$$\text{Propagation delay } (t_p) = 0.35(\tau_r + \tau_f) \quad (9)$$

$$\text{Maximum signal frequency } (f_{\max}) = 1/(t_r + t_f) \quad (10)$$

(ii) Worst case when 1 *n*-MOS On and 1 *n*-MOS Off

$$\text{Total } R_{\text{on}} = (R_{\text{Channel on-state}}) \quad (11)$$

$$\text{Fall time constant } (\tau_f) = \text{Total } R_{\text{on}} \times C_{\text{total}} \quad (12)$$

$$\text{Fall time } (t_f) = 2.2 \times \tau_f \quad (13)$$

$$\text{Propagation delay } (t_p) = 0.35(\tau_r + \tau_f) \quad (14)$$

$$\text{Maximum signal frequency } (f_{\max}) = 1/(t_r + t_f) \quad (15)$$

The theoretical best case value of output low voltage, V_{OL} of nano-MOSFET loaded n-type nano-MOSFET NOR logic gate is given by

$$V_{OL} = \frac{(R_{channel\ at\ on\text{-}state}) \div 2}{((R_{channel\ at\ on\text{-}state}) \div 2) + R_{Load}} \times V_{DD} \quad (16)$$

Meanwhile, the theoretical worst-case value of output low voltage, V_{OL} of nano-MOSFET loaded n-type nano-MOSFET NOR logic gate is given by

$$V_{OL} = \frac{R_{channel\ at\ on\text{-}state}}{R_{channel\ at\ on\text{-}state} + R_{Load}} \times V_{DD} \quad (17)$$

The dynamic power is obtained from the below equation

$$P = aCfV_{DD}^2 \quad (18)$$

The activity coefficient is *a*, the capacitance at the output node is *C*, the frequency of switching is *f*, and the voltage supply is V_{DD} [25-27].

RESULT AND DISCUSSION

Currently, nano-MOSFET semiconductor devices operate in a quasi-ballistic transport region between the drift-diffusion and ballistic regime. Figures 4 to 7 show the schematic circuit diagrams for all four logic families of the NOR gate.

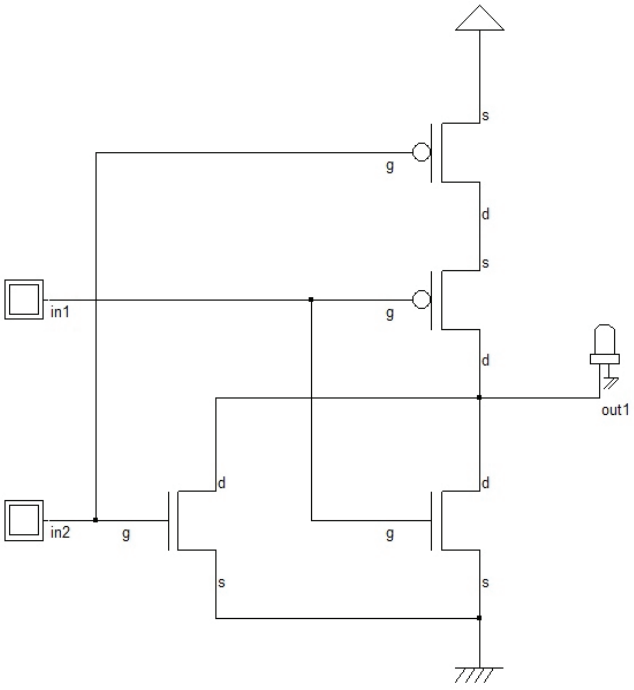


Figure 4 Two inputs nano-CMOS NOR logic circuit

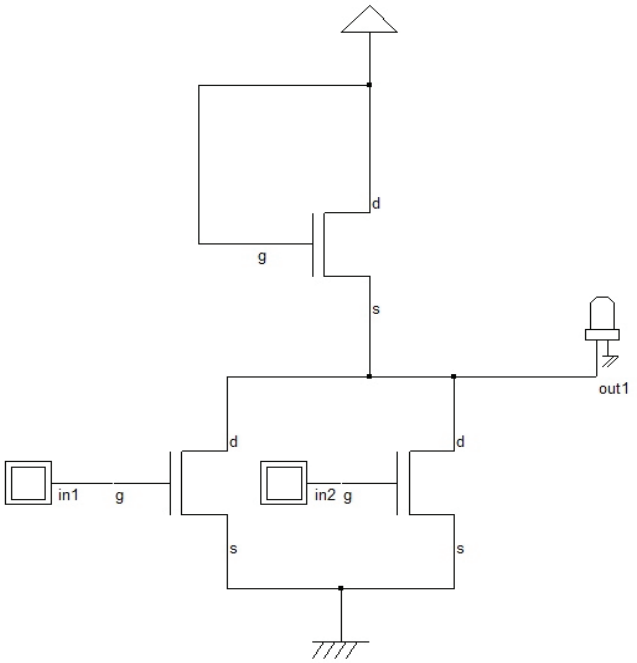


Figure 5 Two inputs nano-MOSFET loaded n-type nano-MOSFET NOR logic circuit

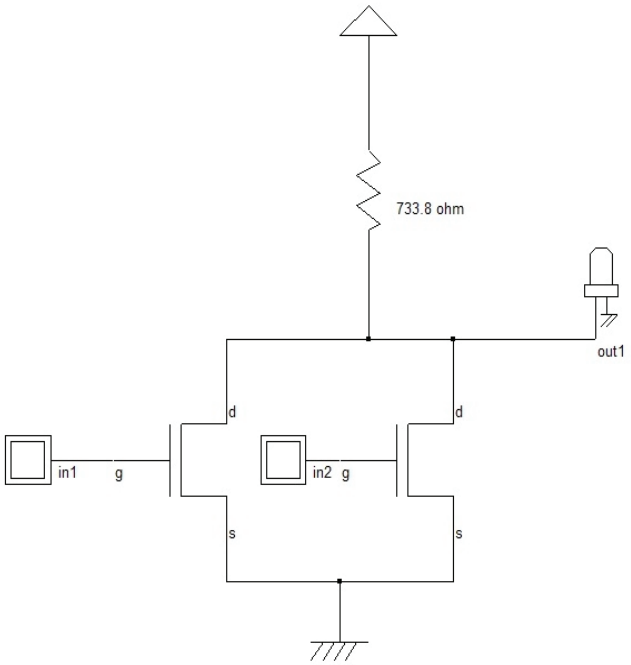


Figure 6 Two inputs resistive loaded nano-MOSFET NOR logic circuit

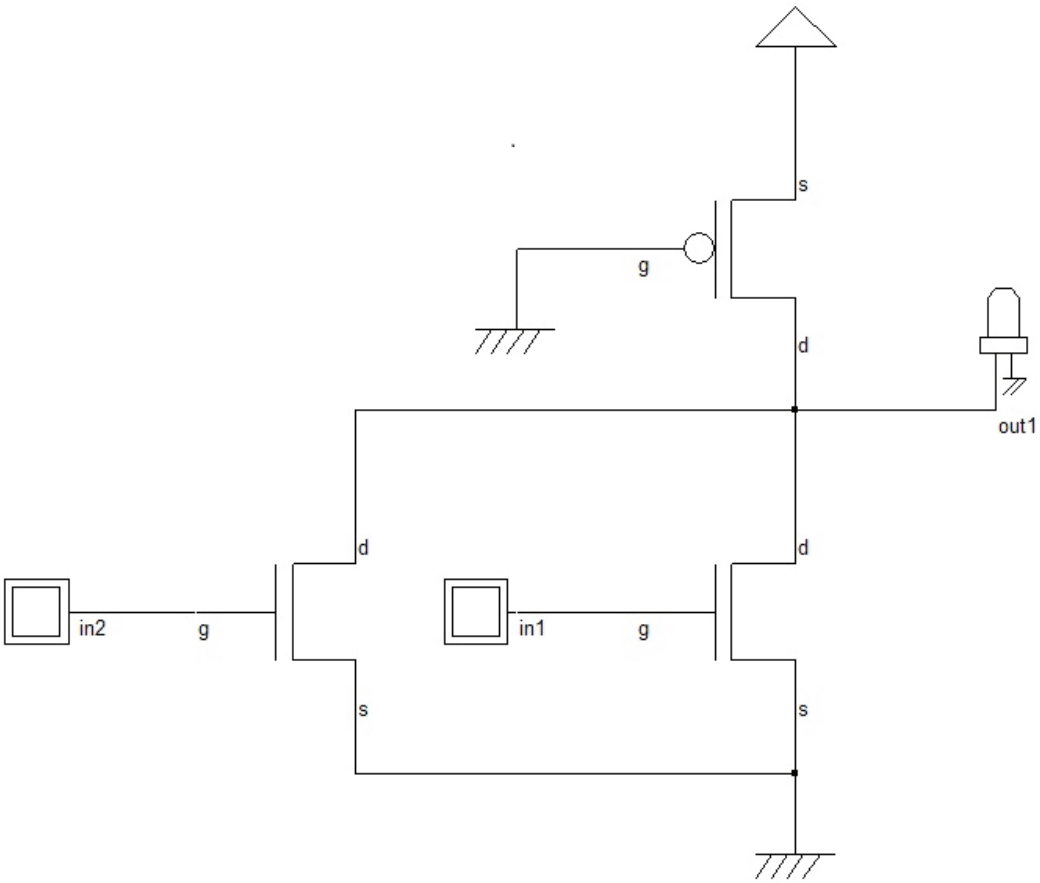
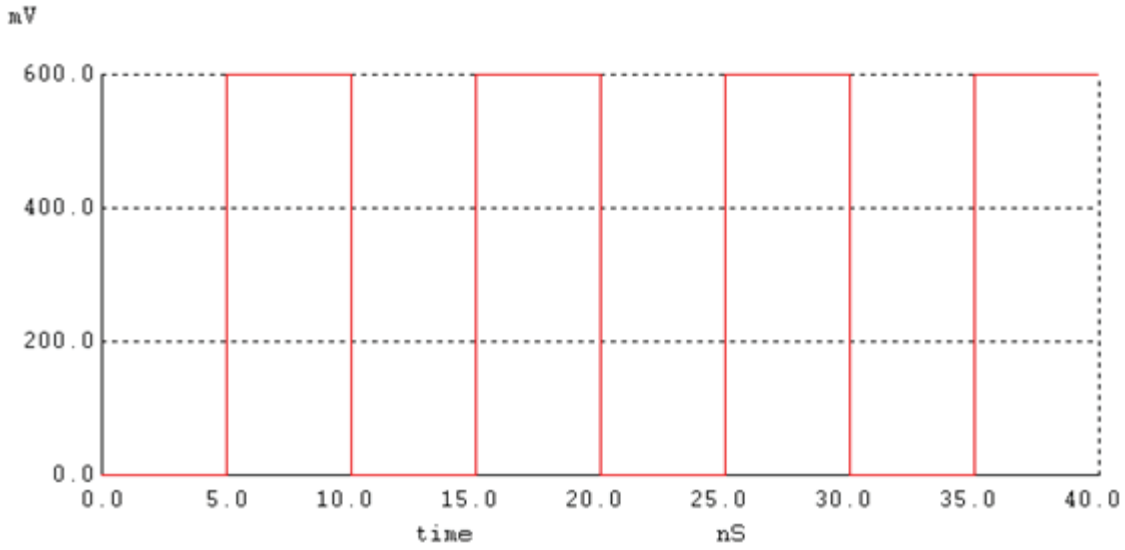


Figure 7 Two inputs pseudo-n-type nano-MOSFET NOR logic circuit

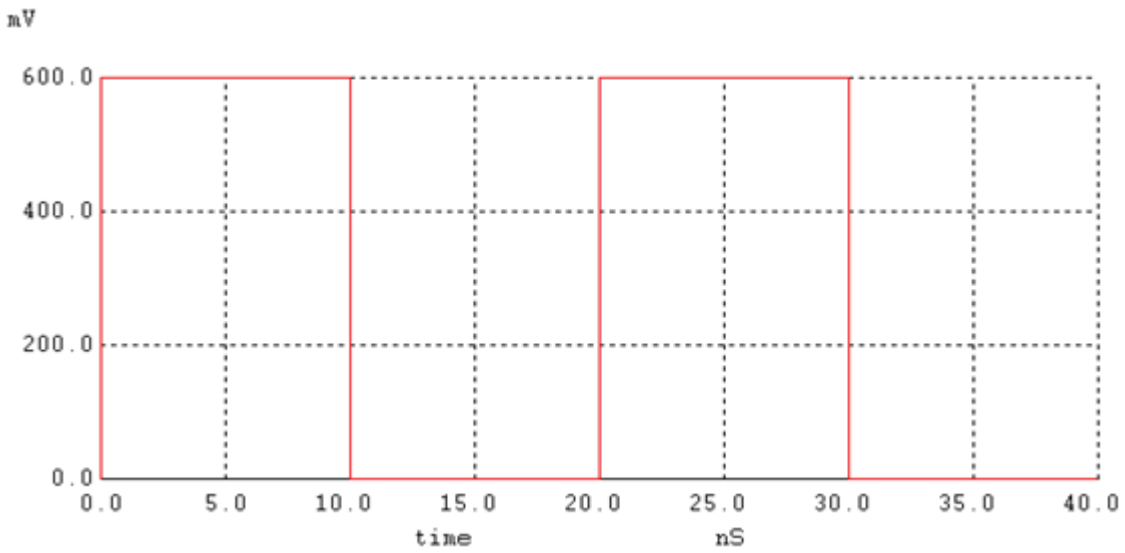
Figure 8(a) and Figure 8(b) show the two input signals to the circuits in Figures 4 to 7. All these two input signals have an amplitude of 0.60 V and a 50% duty cycle. Their frequencies are chosen to be 1×10^8 Hz and 5×10^7 Hz, respectively, because these values are below the maximum signal frequency of around 7.3×10^{11} Hz.

Figure 9, Figure 10, Figure 11, and Figure 12 are the output signals of circuits in Figure 4, Figure 5, Figure 6, and Figure 7, respectively. All these output waveforms showed correct logical NOR operation as in Table 4.

Figure 10 is the output signal of the logic circuit Figure 5, with an amplitude of 0.4 V because of the 0.20 V threshold voltage loss at the load nano-MOSFET, which acts as an n-type pass transistor [28-29]. Figure 11 signal has an amplitude of 0.60 V, and it is the output signal of the logic circuit in Figure 6. The pseudo-n-type nano-MOSFET logic gate has p-type nano-MOSFET with L = 10 nm and



(a) First input signal



(b) Second input signal

Figure 8 Input signals to all four NOR logic circuits

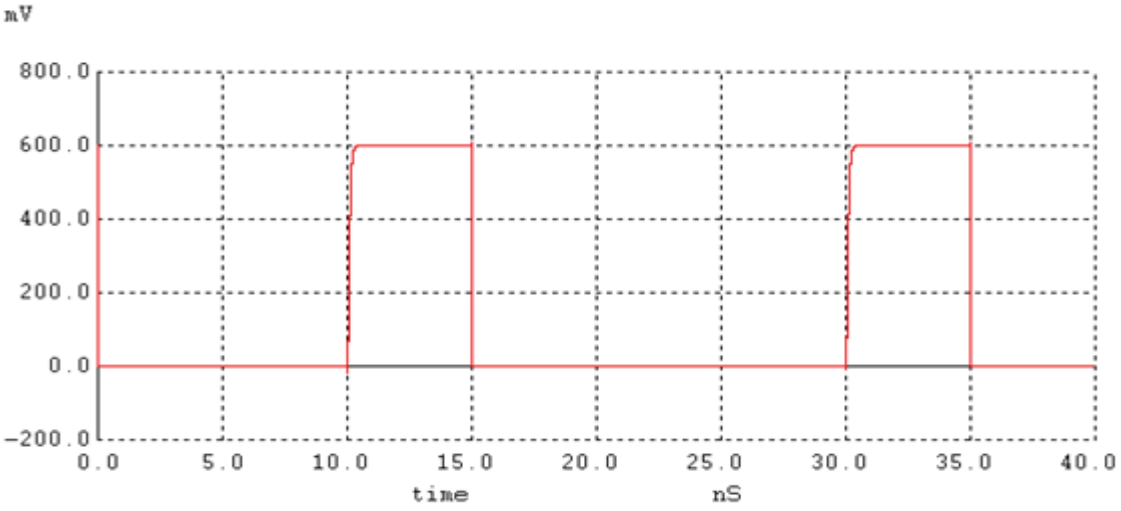


Figure 9 Output signal of nano-CMOS NOR logic circuit

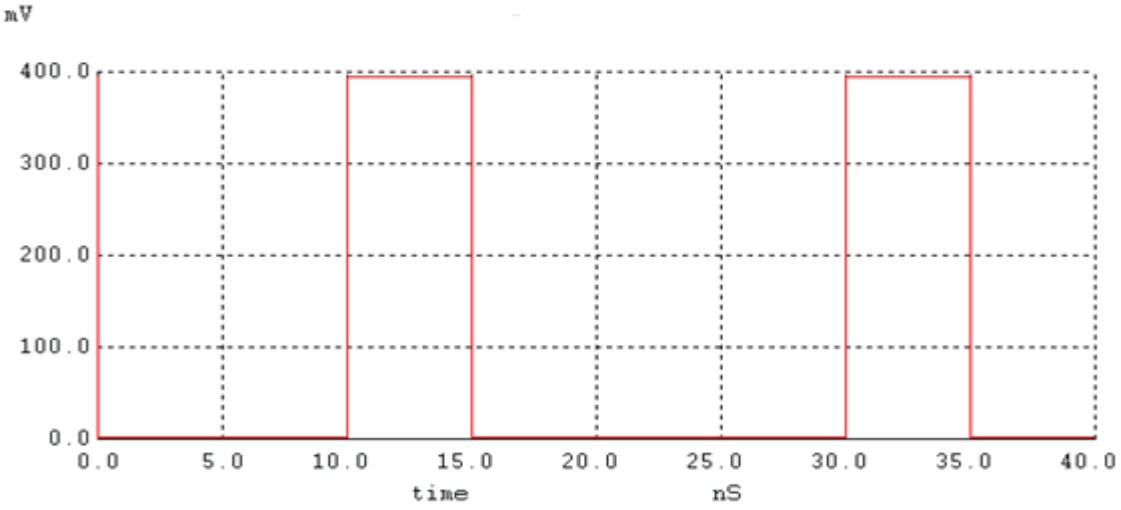


Figure 10 Output signal of nano-MOSFET loaded nano-MOSFET NOR logic circuit

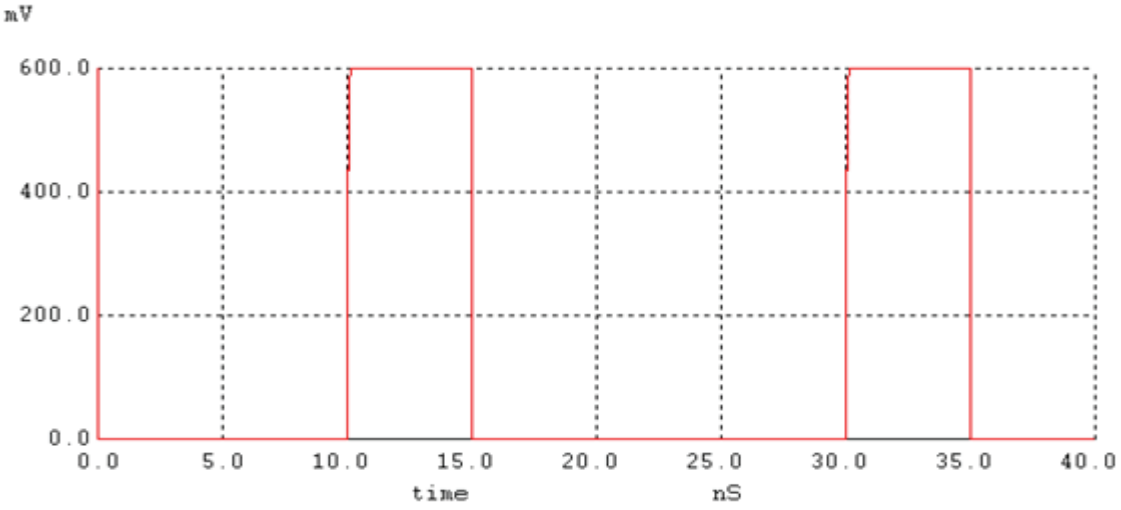


Figure 11 Output signal of resistive loaded nano-MOSFET NOR logic circuit

W = 125 nm, whereas n-type nano-MOSFET with L = 10 nm and W = 250 nm. To reduce output low voltage V_{OL}, the criteria (W/L)n ≥ 2(W/L)Load must be met.

Figure 12 is the output signal of the logic circuit in Figure 7. Its output low voltage is not zero compared with other output waveforms because the pseudo PMOS at the load is always turned ON. This situation caused current still flow during low output state, and so a low output voltage is observed even though during logic 0 output state.

To study the transient response for the logic circuit in Figure 5, two input signals with periods 10 ps and 20 ps are used, and Figure 13 indicates the output result. Signal periods of 10 ps and 20 ps are chosen to measure the rise time and fall time. Rise time and fall time are due to the charging circuit and discharging circuit, respectively. Rise time is defined between 10% and 90% interval of output signal rising edge, whereas fall time is taken between 90% to 10% interval of output signal falling edge. The simulated rise time is 2.231 ps, and the simulated fall time is 0.308 ps which is equivalent to 6 ps pulse width (30% duty cycle). The theoretical calculated best-case propagation delay is 35.9 fs, as tabulated in Table 2. The theoretical calculated worst-case propagation delay is 36.9 fs, as tabulated in Table 2. The simulated propagation delay is 107.1 fs as measured from the WinSpice

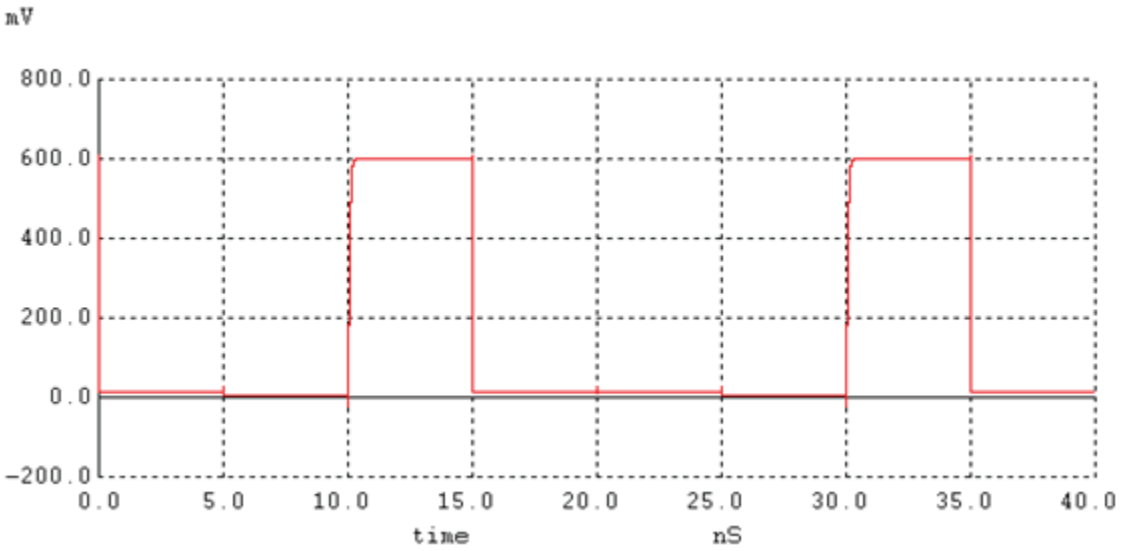


Figure 12 Output signal of pseudo-n-type nano-MOSFET NOR logic circuit

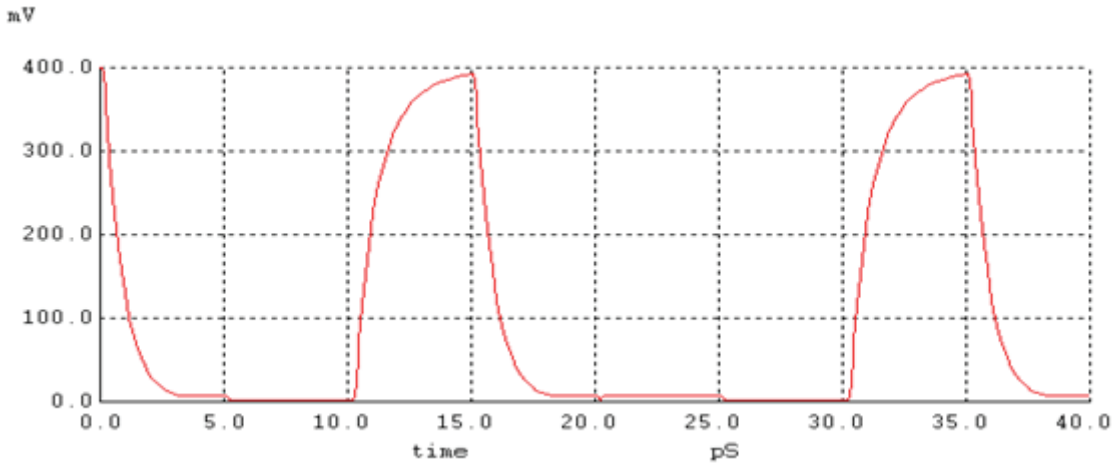


Figure 13 Transient output signal of nano-MOSFET loaded nano-MOSFET NOR logic circuit

output result. Therefore, the theoretical best case switching speed is 2.97 times that of the simulated value.

On the other hand, the theoretical worst-case switching speed is 2.91 times that of the simulated value. From Table 2, the best-case maximum frequency of operation is around 732 GHz, whereas the worst-case maximum frequency of operation is around 729 GHz. The simulated maximum frequency of operation is 394 GHz. The percentage of error between the simulated maximum frequency of operation and the best case maximum frequency of operation values is 46.2%. The percentage of error between the simulated maximum frequency of operation and the worst-case maximum frequency of operation values is 46%. The difference between the simulated and theoretical frequency of operation is that the quasi-ballistic transport model is used in the theoretical calculation.

In contrast, in Winspice simulation, a quantum corrected drift-diffusion model is used. Scattering events are more evident in the quantum corrected drift-diffusion model than the quasi-ballistic transport model. When electron flows through silicon channel with quantum corrected drift-diffusion model, electron encountered many collisions with scattering centers. This causes an electron to take longer to travel from source to drain compared with electron flow with a quasi-ballistic transport model. So, the theoretical quasi-ballistic model has a shorter delay and hence faster frequency. Thus, high speed NOR logic gate designed with 10 nm nano-MOSFET has been achieved. In literature [11], 45 nm MOSFET logic gates have a typical propagation delay of 8.72 ps. Compared with the simulated and best-case theoretical calculated propagation delays, which are 0.1071 ps and 0.0359 ps, respectively, as studied in this paper, the NOR logic gate is designed using 10 nm nano-MOSFET is faster in switching speed. So, higher-speed logic gates can be realized by downscaling of nano-MOSFET [10].

From Figure 13, the simulated best-case output low voltage V_{OL} is 1.5625 mV, whereas the theoretical best case calculated value of V_{OL} is 14.4 mV as derived from equation (16). The ratio between theoretical best case V_{OL} value to simulated V_{OL} is 9.216 times. From Figure 13, the simulated worst-case output voltage VOL is 3.125 mV, whereas the theoretical worst-case calculated VOL value is 28.2 mV as derived from equation (17) [30]-[32]. The ratio between theoretical best worst V_{OL} value to simulated V_{OL} is 9.024 times. Timing response characteristics are tabulated in Table 5. From [19], the propagation delay of the logic gate with structural design T_{Si} = 60 nm W = 1 µm, L = 120 nm MOSFET is typically 3.534 ps. So, it is evident that the10 nm nano-MOSFET NOR logic gate improved 33 times in speed.

Table 6 tabulates the power dissipation for four different NOR logic gates calculated using equation (18) with a = 0.1875. When compared with logic gate

Table 5 Simulated value timing characteristics of NOR gate

WinSpice Simulation Results Using Model Level MOS6 (10% and 90% Points)				
Logic Gates	**Rise Time (t_r)**	**Fall Time (t_f)**	**Propagation Delay (t_p)**	**Maximum Operating Frequency (f_{max})**
NOR	2.231×10^{-12} s	30.760×10^{-14} s	1.071×10^{-13} s	3.940×10^{11} Hz

Table 6 Power dissipation of four logic families for NOR logic gate

	Nano-CMOS NOR	**Nano-MOSFET Loaded NOR**	**Resistive Loaded NOR**	**Pseudo nano-MOSFET NOR**
Dynamic Power (Watts)	1.691×10^{-6}	9.536×10^{-7}	8.829×10^{-7}	1.303×10^{-6}
Voltage Supply (Volts)	0.6	0.6	0.6	0.6
Frequency of Switching (Hertz)	1×10^{11}	1×10^{11}	1×10^{11}	1×10^{11}

designed using MOSFET with W = 1 µm, L = 120 nm, and T_{Si} = 60 nm, which has a downscaled power dissipation of 140.9 µW range as reported in [19], all four logic families NOR gates showed power reduction during downscaling of nano-MOSFET to nanometer regime. The power reduction for nano-CMOS, nano-MOSFET loaded, resistive loaded, and pseudo-nano-MOSFET NOR logic circuits is 83, 148, 160 108, respectively when benchmarked against reference [19]. THE Nano-CMOS NOR logic circuit showed the highest power dissipation because switching nano-MOSFETs is the highest, followed by pseudo-nano-MOSFET NOR logic circuit save one nano-MOSFET when compared to nano-CMOS NOR logic. The power dissipation of the pseudo-nano-MOSFET NOR logic circuit is the second-highest because the pseudo-PMOS is always ON. The third highest power dissipation NOR logic circuit is the nano-MOSFET loaded NOR logic circuit because there is a small voltage drop across the load pass transistor. The lowest power dissipation NOR logic circuit is the resistive loaded NOR logic circuit because the load is purely resistive.

CONCLUSION

In this simulation study, it has been shown that downscaling of nano-MOSFET has the advantages of achieving lower power dissipation and faster speed logic gates. From this paper, nano-MOSFET NOR logic circuits with 10 nm design technology have shown a power reduction of 148 times and a propagation delay improvement of 33 times when compared against a typical 120 nm MOSFET logic. At the same time, logical operations are preserved during downscaling. These advantages are essential in implementing modern consumer electronics products using downscaled nano-MOSFETs to quickly process large amounts of data and have long battery life.

REFERENCES

[1] R. Hosseini & N. Teimuorzadeh, "Simulation study of circuit performance of GAA silicon nanowire transistor and DG MOSFET", *Physical Review & Research International,* 3, 4, pp. 568-576, 2013.

[2] P.A.G. Sankar & K. Udhayakumar, "MOSFET-like CNFET based logic gate library for low-power application: A comparative study", *Journal of Semiconductors,* 35, 7, 2014.

[3] U. Wulf, M. Krahlisch, & H. Richter, "Scaling properties of ballistic nano-transistors", *Nanoscale Research Letters,* 6, p. 365, 2011.

[4] P. Shrivastava & S. Akashe, "Design and analysis of leakage current and delay for double gate MOSFET at 45 nm in CMOS technology", In *2013 7th International Conference on Intelligent Systems and Control (ISCO)* (pp. 301-306), IEEE, 2013.

[5] A.A. Ziabari, M. Charmi, & H.R. Mashayekhi, "The impact of body doping concentration on the performance of nano DG-MOSFETs: A quantum simulation", *Chinese Journal of Physics*, 51, 4, pp. 844-853, 2013.

[6] C. Jeong, D. Antoniadis, & M.S. Lundstrom, "On backscattering and mobility in nanoscale silicon MOSFETs", *IEEE Transactions on Electron Devices,* 56, 11, pp. 2762-2769, 2009.

[7] M. Baldo, "Introduction to nanoelectronics", *MIT Open Course Ware Publication*, 2011.

[8] G.W. Hanson, "Fundamentals of nanoelectronics", *Pearson International Edition*, 2008.

[9] Microsystem Technologies, "Design of 4 nm MOSFET and its applications", *Springer Technical Paper*, 2018.

[10] K. Navi, M. Rashtian, A. Khatir, P. Keshavarzian, & O. Hashemipour, "High speed capacitor-inverter based carbon nanotube full adder", *Nanoscale Research Letters,* 5, pp. 859-86, 2010.

[11] M.L.P. Tan, G. Lentaris, & G.A.J. Amaratunga, "Device and circuit-level performance of carbon nanotube field-effect transistor with benchmarking against a nano-MOSFET", *Nanoscale Research Letters,* 7, p. 467, 2012.

[12] H.C. Chin, C.S. Lim, W.S. Wong, & M.L.P. Tan, "Enhanced device and circuit-level performance benchmarking of graphene nanoribbon field-effect transistor against a nano-MOSFET with interconnects", *Journal of Nanomaterials,* 2014, Article ID 879813, 2014.

[13] A. Verma, A. Mishra, & P. Mishra, "Scaling of dimensions and gate capacitances of MOSFET", *International Journal of Advanced Research in Computer Engineering & Technology (IJARCET)*, 1, 9, November 2012.

[14] R. Gupta, B. Tutuianu, & L.T. Pileggi, "The Elmore delay as a bound for RC trees with generalized input signals", *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems,* 16, 1, pp. 95-104, 1997.

[15] Y. Li & C.-H. Hwang, "High-frequency characteristic fluctuations of nano-MOSFET circuit induced by random dopants", *IEEE Transactions on Microwave Theory and Techniques,* 56, 12, pp. 2726-2733, 2008.

[16] M.-H. Han, Y. Li, & C.-H. Hwang, "The impact of high-frequency characteristics induced by intrinsic parameter fluctuations in nano-MOSFET device and circuit", *Microelectronics Reliability,* 50, pp. 657-661, 2010.

[17] A.A.A. Nasser, M.H. Aly, R.A. Abdel Rassoul, A. Khourshed, "Performance of near-ballistic limit carbon nano-transistor (CNT) circuits", *ICCTA,* pp. 175-182, 2011.

[18] H.F.A. Hamed, S. Kaya, & J. A. Starzyk, "Use of nano-scale double-gate MOSFETs in low-power tunable current mode analog circuits", *Analog Integr Circ Sig Process,* Doi: 10.1007/s10470-008-9134-4, 2008.

[19] K. Naskar, C.J.C. Singh, & S.K. Sarkar, "Analytical modeling of SON MOSFET and realization inverter circuit for high speed and ultra dense low power circuits", *Journal of Nano- and Electronic Physics*, 4, 2, 02023(5pp), 2012.

[20] R. Prasher, D. Dass, & R. Vaid, "Performance of a double gate nanoscale MOSFET (DG-MOSFET) based on novel channel materials", *Journal of Nano- and Electronic Physics*, 5, 1, 01017(5pp), 2013.

[21] O.C. Yee, "Device-circuit level simulation study of three inputs complex logic gate designed using nano-MOSFETs", *Applications of Modelling and Simulation*, 3, 1, pp. 1-10, 2019.

[22] O.C. Yee & L.S. King, "Simulation study on different logic families of NOT gate transistor level circuits implemented using nano-MOSFETs", *Journal of Telecommunication, Electronic and Computer Engineering*, 8, 5, pp. 61-67, 2016.

[23] O.C. Yee & L.S. King, "Study of timing characteristics of NOT gate transistor level circuit implemented using nano-MOSFET by analyzing sub-band potential energy profile and current-voltage characteristic of quasi-ballistic transport", *World Journal of Nano Science and Engineering*, 2016, 6, pp. 177-188, 2016.

[24] O.C. Yee & L.S. King, "Nano-MOSFETs implementation of different logic families of two inputs NAND gate transistor level circuits: A simulation study", *Jurnal Teknologi*, 79, 7, pp. 41-49, 2017.

[25] Z. Ren, "Nanoscale MOSFETs: Physics, simulation and design", *Ph.D. Dissertation*, Purdue University, 2001.

[26] M. Lundstrom, "Notes on the ballistic MOSFET", *Network for Computational Nanotechnology, Purdue University*, 2005.

[27] R. Kim & M. Lundstrom, "Notes on fermi-dirac integrals", *Network for Computational Nanotechnology, Purdue University*, 2011.

[28] O.C. Yee & L.S. King, "Simulation study on the electrical performance of equilibrium thin-body double-gate nano-MOSFET", *Jurnal Teknologi,* 76, pp. 87-95, 2015.

[29] O.C. Yee & L.S. King, "Simulation study of 2d electron density in primed and unprimed subband thin-body double-gate nano-MOSFET of three different thicknesses and two temperature states", *International Journal of Nanoelectronics and Materials,* 9, pp. 67-84, 2016.

[30] S.K. Sinha & S. Chaudhury, "Simulation and analysis of quantum capacitance in single-gate MOSFET, double-gate MOSFET and CNTFET devices for nanometer regime", *IEEE* 978-1-4673-4700-6, 2012.

[31] A. Islam & K. Kalna, "Analysis of electron transport in the nano-scaled si, SOI and III-V MOSFETs: si/sio_2 interface charges and quantum mechanical effects", *IOP Conference Series: Materials Science and Engineering*, 2019.

[32] A.E. Atamuratov, A. Yusupov, Z.A. Atamuratova, J.C. Chedjou, & K. Kyamakya, "Lateral capacitance-voltage method of nanoMOSFET for detecting the hot carrier injection", *Applied Sciences*, 2020.